REMARKS

Initial remarks:

Applicant initially notes with appreciation the Examiner's indication in the July 16 Office Action that Claims 13-15 would be allowable if appropriately rewritten. In this regard, new Claims 43-45 include the limitations of dependent Claims13-15, respectively, rewritten in independent form and are therefore believed to be in condition for allowance and such disposition is respectfully requested.

Drawing objections:

The Examiner has objected to the drawings under 37 C.F.R. 1.83(a). Enclosed herewith is a proposed corrected FIG. 3C and Applicant respectfully submits that in view of the proposed corrections the objection to the drawings should be withdrawn. In this regard, among other features, the proposed corrected drawing illustrates the first dielectric layer 30 comprising a lower layer 30A of thermal oxide and an upper layer 30B of silicon nitride, the second dielectric layer 50, the first electrically conductive layer 40, and the second electrically conductive layer comprised of two separately deposited layers 60, 70 of doped polysilicon.

Claim rejections under 35 U.S.C. § 112, first paragraph:

In the July 16 Office Action, the Examiner rejected Claims 3-5, 25-27 and 35-37 under 35 U.S.C. § 112, first paragraph, contending that such claims include "subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." Applicant respectfully submits that, as stated in the July 16 Office Action, Applicant cannot understand the basis for the rejection and respectfully requests that such rejection be withdrawn or clarified in a subsequent non-final Office Action so that Applicant can properly respond. In this regard, in the July 16 Office Action, the Examiner states:

> The specification, specify in figure 3C, is silent regarding "the first dielectric layer comprises lower and upper layers, and a second dielectric layer overlying the conductive lines and the first dielectric layer", "a shielded electrically conductive line, claim 33, line 1", and "a second dielectric layer, claims 4 and 36, line 2", "a first

and a second conductive layers of doped polysilicon, and the second conductive layer comprises two separately deposited layers of doped polysilicon, claims 6-8", and "conductive line being surrounded by dielectric material along a lengthwise extent of each said electrically conductive line, claim 24, lines 4-5".

A review of the pending claims indicates that none of Claims 3-5, 25-27 or 35-37 recite the phrase "the first dielectric layer comprises lower and upper layers, and a second dielectric layer overlying the conductive lines and the first dielectric layer" and the Examiner has not identified for Applicant in which of the Claims rejected under the first paragraph of 35 U.S.C. § 112 such language is included. Further, the Examiner refers to Claims 6-8, 24 and 33, but such Claims are not included in the listed claims rejected under 35 U.S.C. § 112, first paragraph, namely claims 3-5, 25-27 and 35-37 and Applicant cannot infer how language attributed by the Examiner to Claims 6-8, 24 and 33 supports a rejection of Claims 3-5, 25-27 or 35-37 under the first paragraph of 35 U.S.C. § 112. As to the "second dielectric layer" in Claim 4, line 2 and Claim 36, line 2, Applicant directs the Examiner to page 9, line 24 through page 10, line 10 of the specification wherein formation of a second dielectric layer is described in detail, clearly demonstrating that Applicant has described the "second dielectric layer" in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, did indeed have possession of the claimed invention.

Claim rejections under 35 U.S.C. § 102(b):

In the July 16 Office Action, the Examiner rejected Claims 1-2, 4-8, 24-26, 28-30, 32, 33-34 and 36-41 under 35 U.S.C. § 102(b) contending such claims are anticipated by United States Patent No. 6,022,787 to Ma. Applicant respectfully disagrees that Ma discloses Applicant's invention as set forth in independent Claims 1, 24 and 33 and respectfully submits that independent Claims 1, 24 and 33, and all claims depending directly or indirectly therefrom are in condition for allowance. As summarized more fully below, in each of independent Claims 1, 24 and 33 there is no intervening electrically conductive layer or structure between the electrically conductive lines and the substrate and the only intervening layer between the electrically conductive lines and the substrate is the first dielectric layer. However, as summarized more fully below, in Ma there is an electrically conductive bottom wall between the conductors and the substrate.

Independent Claim 1 is directed to a shielded multi-conductor interconnect bus including a substrate, a first dielectric layer overlying and supported by at least a portion of the substrate, a plurality of parallel electrically conductive lines formed on the first dielectric layer, a plurality of parallel electrically conductive walls formed on the first dielectric layer, each electrically conductive wall including an upper section extending vertically above the level of the electrically conductive lines, and an electrically conductive shield formed in a spaced relation above the electrically conductive lines and in contact with the upper sections of the electrically conductive walls. Further, in accordance with the limitations of Claim 1 there is no intervening electrically conductive layer between the plurality of parallel electrically conductive lines and the substrate, and the electrically conductive lines and the electrically conductive walls are arranged in pattern wherein one of the electrically conductive walls is located between sets of the electrically conductive lines, with each set of electrically conductive lines including at least one of the electrically conductive lines.

Independent Claim 24 is directed to a shielded multi-conductor interconnect bus including a substrate, a plurality of electrically conductive lines formed on the substrate, each electrically conductive line being surrounded by dielectric material along a lengthwise extent of each electrically conductive line, an electrically conductive shield overlying and spaced above the electrically conductive lines, and a plurality of electrically conductive walls formed on the substrate, each electrically conductive wall being in contact along a lower section thereof with the substrate and along an upper section thereof with the electrically conductive shield. Further, in accordance with the limitations of Claim 24, there are no intervening electrically conductive structures formed between each electrically conductive line and the substrate, and the electrically conductive lines and the electrically conductive walls are arranged in pattern wherein one of the electrically conductive walls is located between sets of the electrically conductive lines, with each set of electrically conductive lines including at least one of the electrically conductive lines.

Independent Claim 33 is directed to a shielded electrically conductive line comprising a substrate, a first dielectric layer overlying and supported by at least a portion of the substrate, an electrically conductive line formed on the first dielectric layer, a pair of parallel electrically conductive walls formed on the first dielectric layer, each electrically conductive wall being located on an opposing side of the electrically conductive line and including an upper section extending above the level of the electrically conductive line, and an electrically conductive

shield formed in a spaced relation above the electrically conductive line and in contact with the upper sections of the electrically conductive walls. Further, in accordance with the limitations of Claim 33, there is no intervening electrically conductive layer between the electrically conductive line and the substrate.

Ma does not disclose the shielded multi-conductor interconnect buses of Claims 1 and 24 or the shielded electrically conductive line of Claim 33. Of particular significance is that in Ma, there is an intervening electrically conductive layer or structure between the conductors and the substrate. In this regard, the single conductor isolation structures of Ma include an enclosure 100 surrounding the isolated conductor 90 having a bottom wall 104 made of highly electrically conductive material. See FIGS. 2 and 7 and Col. 4, line 65 through Col. 5, line 30 of Ma. The single level multiple conductor isolation structure of Ma includes an enclosure 190 surrounding the isolated conductors 191-193 having a bottom wall 196. See FIG. 17 and Col. 10, lines 6-31 of Ma. The multiple level multiple conductor isolation structure of Ma includes an enclosure 160 having four cells 161-164 arranged in a two-by-two matrix to isolate conductors 171-174 from one-another and other conductors outside of enclosure 160. Enclosure 160 includes a lower conductive layer 165 that is common to the bottom cells 161-162. See FIG. 16 and Col. 9, lines 32-54 of Ma.

A number of advantages are achieved with the shielded multi-conductor interconnect buses of Claims 1 and 24 or the shielded electrically conductive line of Claim 33 as compared with the isolation structures disclosed in Ma. One advantage is that the vertical topography of the shielded multi-conductor interconnect buses of Claims 1 and 24 or the shielded electrically conductive line of Claim 33 can be less than that of Ma since an intervening layer of electrically conductive material between the conductors and the substrate and layer of dielectric material separating the conductors from the intervening layer of electrically conductive material are not required. Including an electrically conductive bottom wall or lower conductive layer between the conductors and the substrate also requires additional fabrication steps as compared to the shielded multi-conductor interconnect buses of Claims 1 and 24 or the shielded electrically conductive line of Claim 33. Having fewer fabrications steps leads to faster fabrication and lower fabrication costs for the shielded multi-conductor interconnect buses of Claims 1 and 24 or the shielded electrically conductive line of Claim 33.

Based upon the foregoing, pending independent Claims 1, 24 and 33, as well as their corresponding dependent claims are allowable over Ma. There is therefore no need to separately address the patentability of each dependent claim and/or the Examiner's interpretation in relation to any of the dependent claims or any of the references of record in relation thereto.

Conclusion:

In view of the foregoing, Applicant believes that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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